Dual N-Channel 24V(S-S) MOSFET

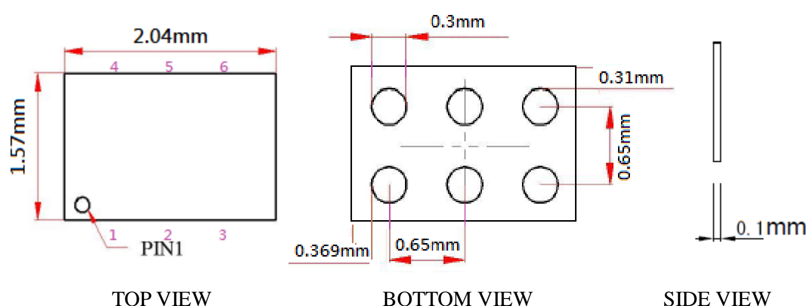
GENERAL DESCRIPTION

The FMW6620DW-G is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as notebook computer power management and other battery powered circuits where Low-side switching , and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- RSS(ON) ≦11.2 mΩ@VGS=4.5V
- RSS(ON) ≦12.0 mΩ@VGS=4.0V
- RSS(ON) ≦12.2 mΩ@VGS=3.8V
- RSS(ON) ≦14.7 mΩ@VGS=3.1V
- RSS(ON) ≦22.5 mΩ@VGS=2.5V
- ESD Protection HBM Class-2
- Low Gate Charge
- Exceptional on-resistance and maximum DC current capability
- MSL=1

PIN CONFIGURATION

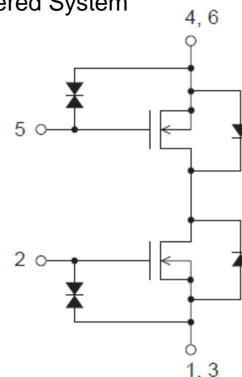


Unless otherwise specified,tolerances:x.xx±0.05(mm)

0.xx±0.03(mm)

APPLICATIONS

- Power Management
- DC/DC Converter
- Load Switch
- Battery Powered System



Ordering Information: FMW6620DW-G (Green product-Halogen free)

Absolute Maximum Ratings (TA=25℃ Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{SS}	24	V
Gate-Source Voltage		V_{GS}	±8	V
Continuous Drain Current	T_A=25℃	I_D	12.4	A
	T_A=70℃		9.9	
Pulsed Drain Current		I_{DM}	50	A
Maximum Power Dissipation	T_A=25℃	P_D	2	W
	T_A=70℃		1.3	
Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	℃
Thermal Resistance-Junction to Ambient *		$R_{\theta JA}$	62.5	℃/W

* Surface mounted on ceramic substrate (5000 mm^2 x 0.8 mm).

Electrical Characteristics (T_J=25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
$V_{(BR)SSS}$	Source-Source Breakdown Voltage	V_{GS}=0V, I_S=1mA	24			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{SS}=10V, I_S=1.2mA	0.35		1.4	V
I_{GSS}	Gate Leakage Current	V_{SS}=0V, V_{GS}=±8V			±1	μA
I_{SSS}	Zero Gate Voltage Source Current	V_{SS}=24V, V_{GS}=0V			1	μA
$R_{SS(ON)}$	Source-Source On-State Resistance[a]	V_{GS}=4.5V, I_S= 3A	5.7	8.2	11.2	mΩ
		V_{GS}=4.0V, I_S= 3A	5.8	8.4	12.0	
		V_{GS}=3.8V, I_S= 3A	5.9	8.7	12.2	
		V_{GS}=3.1V, I_S= 3A	6.3	9.7	14.7	
		V_{GS}=2.5V, I_S= 3A	7.0	12.5	22.5	
$V_{F(S-S)}$	Forward Source-Source Voltage	I_S=6A, V_{GS}=0V			1.2	V

Notes: a. pulse test: pulse width≦ 300us, duty cycle≦ 2%, Guaranteed by design, not subject to production testing.

b. Force mos reserves the right to improve or change product design, functions, reliability, qualified manufacturer without notice.

* If RSS(on) measurement is performed with the single device mounted on 1 in2 FR-4 board with 2oz, RSS(on) max. value refers to *On test board.

DYNAMIC						
Q_g	Total Gate Charge	V_{SS}=6V, V_{GS}=4V, I_D=4A		40.4		nC
Q_{gs}	Gate-Source Charge			11		
Q_{gd}	Gate-Drain Charge			15.7		
C_{iss}	Input Capacitance	V_{SS}=6V, V_{GS}=0V F=1MHz		2518		pF
C_{oss}	Output Capacitance			412		
C_{rss}	Reverse Transfer Capacitance			194		
$t_{d(on)}$	Turn-On Delay Time	V_{SS}=6V, R_L =1.5Ω V_{GS}=4V,R_G=3.3Ω I_S=4A		0.5		μs
t_r	Turn-On Rise Time			0.88		
$t_{d(off)}$	Turn-Off Delay Time			1.27		
t_f	Turn-Off Fall Time			5.19		

Notes: Switching time test circuit and waveform are based on MIL-STD-750E Measuring methods

Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time

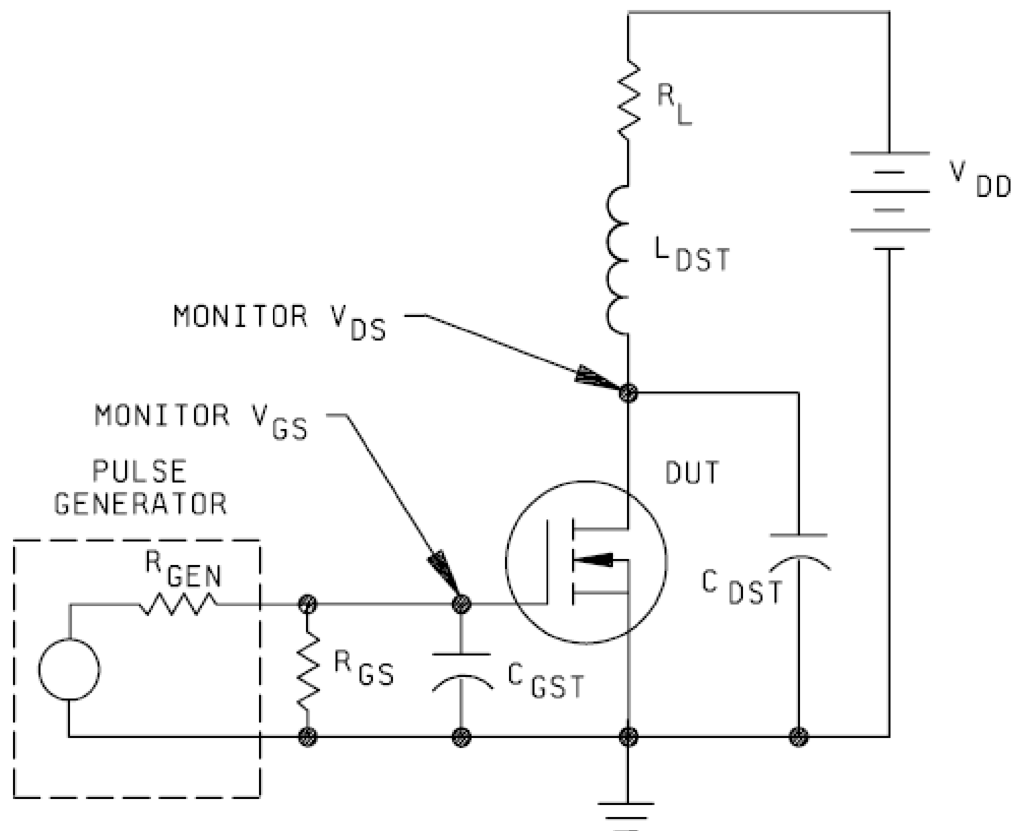


Fig.1 Switching time test circuit.

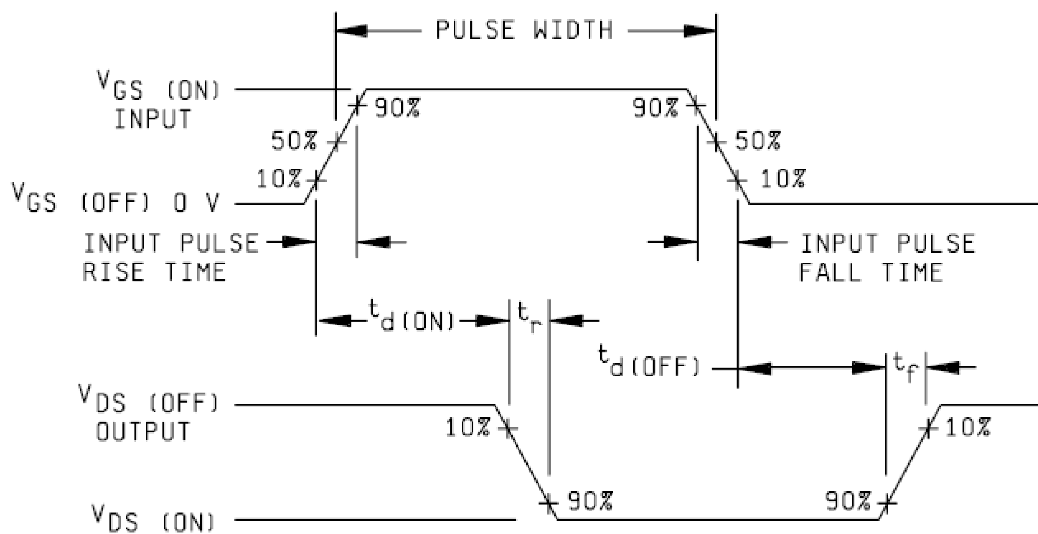


Fig.2 Switching time waveforms.